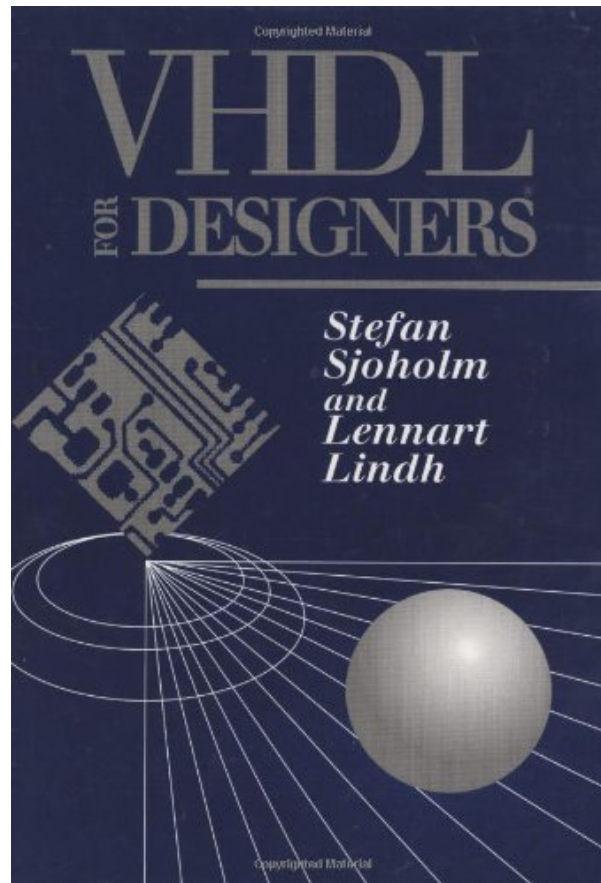
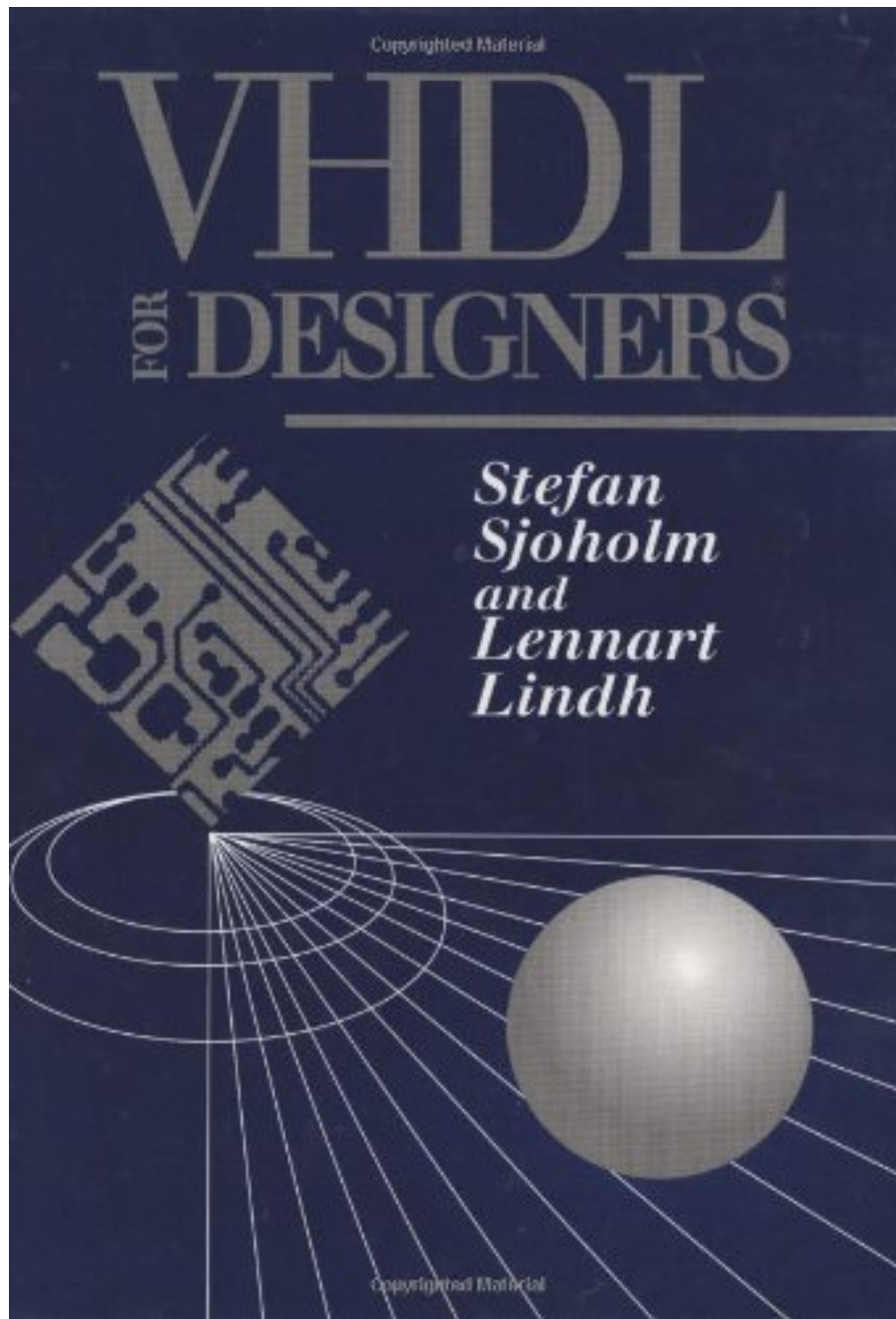


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A practical guide to help electronics designers and students make the most of VHDL with the latest, most widely-used design tools available. This book presents both the professional and academic side of designing with VHDL, and shows how to take full advantage of VHDL with today's design tools. It contains many worked examples developed with Synopsys, Mentor Graphics and ViewLook tools. It reviews concurrent, sequential and structural VHDL, RAM and ROM development, state machines, and RTL synthesis. Test methodologies and rapid prototyping are covered, as well as examples of quality design and common errors to avoid. End-of-chapter exercises and laboratories are included throughout. For both engineering professionals and students interested in using VHDL as effectively as possible in their environments.

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The specific goal of VHDL for Designers is not only to teach VHDL but also to describe how to use VHDL when designing an electronic system with modern design tools. The synthesis tools Synopsys, Mentor Graphics and ViewLogic are used.

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Too much design, not enough VHDL

By wiredweird

I guess I was looking for a different book. I'm already quite familiar with hardware design, so I wasn't looking for a book to teach me that. I already have the IEEE VHDL standard document, but that's like reading a phone book. I wanted a readable handbook of the VHDL language - I never found that, so I settled for "VHDL for Designers" instead.

I come from a software background, programming in the large. I was looking for a book to teach me the language. For a programmer, that includes the record types (like C structs), 'generate' and 'generic' for parameterizing my design, recommended style for combining operator overloads with component definitions, proper use of libraries, packages, and multiple architectures, and so on.

This book is just the baby steps of VHDL. It's very focussed on its examples, and seems to give just enough VHDL for each example. It's OK for design at the "Hello world" level, but not much past that. It has most of the basic language constructs, but shallow discussion of them. The organization doesn't really lend itself to use as a language handbook.

Still, it does cover the basics. I'll just have to tough it out for the rest of the language. I still use the book, but I'm still looking for a better one.

9 of 12 people found the following review helpful.

A very good book in VHDL

By A Customer

This is the book one should have who is doing something or anything in VHDL. Previously I had two books but those were filled with unnecessary explanation and nonsense examples. This book explain the facts to the point with plenty of examples. I think that it best for the startup and also for the experienced peoples for their reference.

1 of 1 people found the following review helpful.

a good book

By Pavel Grishin

I learned VHDL and developed a number of working designs using this book. It features many examples which may be used as skeleton for design blocks.

It does not teach theory of digital design; it demonstrates how to implement design in VHDL so that it can be synthesized.

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